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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicants	:	Rakesh Malik and Puneet Goel
Application No.	:	09/807,500
Filed	:	June 11, 2001
For	:	AREA EFFICIENT REALIZATION OF COEFFICIENT ARCHITECTURE FOR BIT-SERIAL FIR, IIR FILTERS AND COMBINATIONAL/SEQUENTIAL LOGIC STRUCTURE WITH ZERO LATENCY CLOCK OUTPUT

Art Unit	:	2171
Docket No.	:	851663.422USPC
Date	:	October 23, 2001

Box PCT
Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Commissioner for Patents:

Prior to an examination on the merits of the case, please amend the above-identified application as follows:

In the Claims:

Please amend claims 5 and 6 to read as follows: For the Examiner's convenience, all claims pending in the application are shown so that the claims may be viewed in their entirety.

1. A filter device comprising logic architecture [A] connected to coefficient lines CLin_0, CLin_1.....CLin_n and/or BLin_0, BLin_1.....BLin_n coming from delay

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